PRECISION SUBNANOSECOND DELAY MEASUREMENTS OF HIGH SPEED DIGITAL INTEGRATED CIRCUITS*

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Abstract

Precise measurements of high speed digital integrated circuit time delays have been performed by a frequency domain technique instead of direct time domain methods. Resolutions to 1 picosecond are possible with absolute accuracies approaching 10 picoseconds. This method uses a PN data comparison with a spring loaded hold down test fixture. It can be used to test a variety of circuit types and can be applied in production environments.

Introduction

A system for providing detailed performance parameters of high speed integrated circuits requires a carefully designed signal source as well as operational considerations in order to obtain a resolution which is consistent with the circuit performance.

The technique used in this system has been chosen such that a one ps resolution along with a measurement uncertainty approaching 10 ps can be obtained. This precision is achieved without the use of variable delay lines and calibration is performed with an ordinary sampling oscilloscope.

Figure 1 illustrates the functional diagram of the test system. The system is designed to provide a 63 bit code as the test data and a reference data corresponding to the correct circuit under test response. The accuracy and resolution is obtained by shifting the test data one bit with respect to the reference data and then making up for this time shift with a delay line corresponding to one bit delay at some predetermined frequency. Relative time shifts of these two signals as well as the clock signal is provided by changing the clock frequency. The threshold at which the circuit response and the reference signal exceeds a predetermined amount of time is detected in a high speed comparator. The frequency at which this threshold occurs corresponds to a well controlled time shift which can be calculated from measured parameters of the test system.

Signal Source

The signal source is a maximal length PN generator with a variable data rate from 50 to 500 Mb/s with data rise times of 0.5 nanoseconds. This generator is a 6 bit high speed shift register with feedback. Data rates are controlled by variation of the clock frequency. The clock source is an externally controlled sweep generator. High speed IC's developed by Motorola's Government Electronics Division are used in the generator.

A PN code was used as data in lieu of other data patterns to permit measurement of true max and min delay times. Delay times for the high speed circuits under test are typically data dependent. While the reasons for this dependency are not under consideration here, a factor likely to produce such dependency is capacitance of the internal device bias source. A change in duty cycle is likely to cause a change in bias threshold which results in a delay change. Previous measurement techniques using ring oscillator type configurations do not address this problem and, therefore, are not valid for precise max and min delay measurements. Use of a PN data stream results in a distribution of delay times from which the max and min times can be extracted.

Principle of Operation

Given that a PN generator is used as a data source a dual channel sampling scope could be used to measure the individual time delays for each bit. However, the time consuming measuring process for max/min values, time base jitter, probe fixturing, and calibration restrict its use primarily to the laboratory.

The test method used to measure the time delays precisely is a simple form of correlation. In general a correlation between two data streams can be represented by

$$R_{xy}(\tau) = \overline{x(t)\, y(t-\tau)}$$

If x(t) is a delayed version of y(t) with a delay of T_D, then R_{xy} will be a maximum for $\tau = T_D$ as τ is varied.

Rather than implement the correlation strictly, a simple comparison is made. Both data outputs are compared with a high speed exclusive-or comparator. As the data streams are shifted in time relative to each other, the point of max alignment can be determined. The actual determination of the time displacement is performed in the frequency domain by relating alignment to the generator clock frequency.

Measurement Method

The output of the PN generator (fig. 2) generates two data streams, test data and reference data. The reference data is delayed by a variable bit time, T_V, and by a fixed delay, T_R. Test data has only a fixed delay, T_T, where $T_T > T_D$ (fig. 3). For no other delays in the data paths test and reference data will be in precise alignment when

$$T_T = T_V + T_R$$

or, $$T_V = T_T - T_R$$

If a delay to be measured, T_x, is inserted in the test data line then,

$$T_T + T_x = T_V + T_R$$

or, $$T_x = T_V + T_R - T_T$$

Now the delay T_x can be determined by making two sets of measurements. The first measurement is made for some element having a known delay such as a short length of line. This has to be done only once. Then,

$$T_T = T_{V_o} + T_R - T_{x_o} \text{ where } T_{x_o} \text{ is known.}$$

$$T_{V_o} = 1/F_o$$

Here F_o is the generator clock frequency for best max or min alignment. This procedure is repeated for the unknown delay.

$$T_{x1} = T_{V1} + T_R - T_T \qquad \text{for unknown delay}$$

$$T_{x1} = I/F_1 + T_R - T_T$$

$$T_T = 1/F_o + T_R - T_{xo} \qquad \text{for known delay}$$

$$T_{x1} = 1/F_1 - 1/F_o + T_{xo}$$

Derivation of the relationship between F_o and F_1 for delay determination implied that exact alignment was necessary. Realistically, the comparator cannot detect perfect alignment. As long as the comparator time threshold is constant, however, the threshold can be greater than 0. Since delay determination is a difference of F_1 and F_o, the time threshold used to specify F_1 and F_o can be other than 0.

Max and min delays are distinguished by a form of PLL. The high speed comparator is followed by a high speed monostable, lo-pass filter, and a sweep generator used as the PN generator clock source. For max delays the sweep generator will sweep up to the point where only the longest delay will be at the comparator threshold and it will be locked at that point. Min delays are found in a similar manner. The generator, however, sweeps down until only the smallest delay will exceed the threshold.

Error Sources

A number of sources of error exist within the system. Coax connections, test fixturing, comparator performance, and oscillator stability are major sources. Use of SMA type connectors and semi-regid coax cable minimize mismatch and connection physical displacement changes. However, reconnection of connectors results in a change in delay parameters by at least several picoseconds.

Two major factors of error in comparator performance are comparator threshold changes due to slight shifts in ambient temperature and input line reflections. Previous data indicates that the threshold change error is about 0.5 ps/^{o}c change in temperature. For a 4^{o}c change in room ambient this will result in about 2 ps error. Line reflections are dependent on how well impedance matching can be done to the comparator in the test fixture. Data indicates that this error is on the order of 11 ps without any fine tuning of the matching.

Oscillator short term stability has been observed to be a maximum of 0.03%. For a frequency range of 150 to 400 MHz this results in a time error of 2 ps.

The test fixture uses a microstrip test circuit board with a spring loaded hold down for the circuit under test. The principle source of error is fixed path length differences. For a path length difference of 100 mils the expected time error is 10 ps. This is time error between pin to pin delay measurements. For a given input pin delay measurement on a single type device lot path difference exists only because of IC insertion position change. Error in this case is less, about 5 ps.

The error terms are summarized in table 1. Two sets of values are shown. The first set of values correspond to those conditions previously mentioned. The second set of values correspond to an optimum condition case. In this case connector change and oscillator instability are a minimum. Also a 1^{o}c change in temperature is assumed. The error terms due to reflections and path length differences are for the case where relative delays are being measured for a lot of one device type.

Results

The results shown in Table 2 were obtained for thruput delay measurements on a high speed S10 flip-flop developed by Motorola. The number of devices in the tested lot was 13. Each device was tested 5 times by retesting the whole lot 5 times. Item 1 is the worst case value found after test completion. Item 2 is the mean value for the distribution of max and min values with the standard deviation given in item 3. Item 4 is the worst case difference found when the devices were retested. Item 5 is the standard deviation for the retested devices.

Conclusions

The indirect frequency domain approach for determining time delays is a test method that can provide additional delay measurement capability. Its chief advantages are that it has high resolution, and that it can be used to quickly determine max and min time delays from a distribution. In addition, it can be applied to a variety of circuit types or time measurement applications, and it can be automated for factory use.

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References

1. C. Ryan, "AC test fixture for high speed digital circuits," Motorola GED technical document, August 1976.

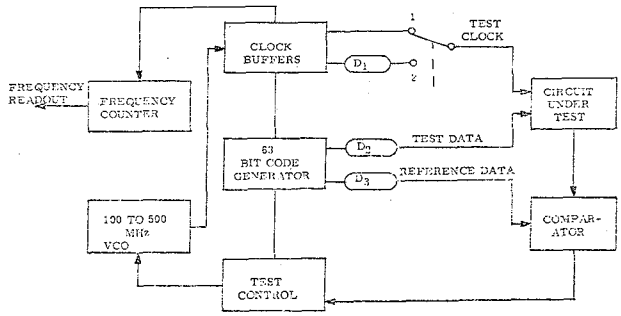

Figure 1. High Speed Circuit Test System

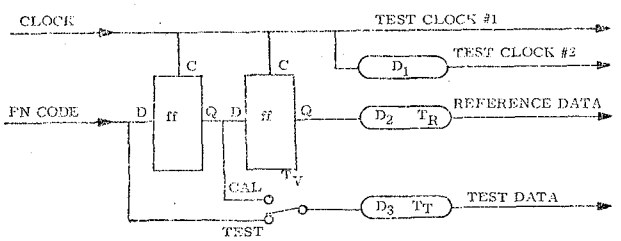

Figure 2. Simplified Diagram of the Signal Source

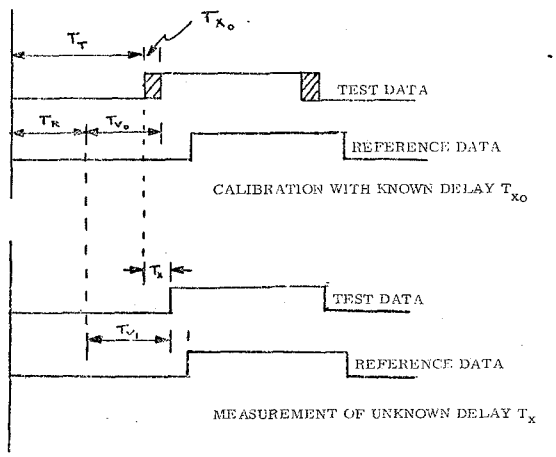

Figure 3. Data Alignment Times

TERM	WORST CASE VALUE (PS)	OPTIMUM CASE VALUE (PS)
CONNECTIONS	2	0
COMPARATOR	13	2
OSCILLATOR	2	1
FIXTURE	10	5
TOTAL WORST CASE	27	8
TOTAL RMS	17	5

Table I. System Error Terms

ITEM NO.	ITEM	MAX PS	MIN PS
1	WORST CASE DELAY	858	566
2	MEAN LOT DELAY	839	585
3	MAX/MIN STD. DEVIATION	22	16
4	WORST CASE RETEST DIFFERENCE	9	4
5	RETEST STD. DEVIATION	4	3

Table 2. S10 Test Results